PAT9102DM-T4QU: Optical Tracking Chip

Product Datasheet

General Description

The PAT9102 is PixArt Imaging's high performance Optical Tracking Chip (OTC), using low power CMOS chip designed specifically for dual axis tracking on surfaces in printer and automation applications. The OTC offers high accuracy with repeated error of 0.15 % over 25 mm of media movement with speeds up to 20 inches per second (ips). The OTC integrates light source and optical chip with built in picture element recognition engine and DSP that provides the host system real-time feedback.

Key Features

- Dual axis tracking chip
- Integrated 16 pin molded lead-frame DIP package
- High accuracy with repeated error of 0.15 % over 25 mm travel distance
- High resolution of 17904 cpi
- Supports Four-Wire Serial Port Interface (SPI)
- External interrupt output for motion detection
- Internal Oscillator – no clock input needed

Applications

- Print media applications
- Scanners
- Machine vision and automation

Key Parameters

Parameter	Value
Supply Voltage (V)	V_{DD}: 3.0 – 3.6 V_{DDIO}: 3.0 – 3.6
LED Supply Voltage (V)	V_{LED}: 3.0 – 3.6
Raw Data Array	32 Col x 32 Row
Interface	4-Wire SPI @ 2 MHz
Repeated Error (%)	0.15 (+/- 0.0375 mm over 25 mm travel distance)
Speed (ips)	20
Acceleration (m/s^2)	4
Resolution (cpi)	17904
Z Height (mm) (Distance from Lens Reference Plane to Tracking Surface)	2.4
Package Type	16 pin molded lead-frame DIP package assembled with lens: 10.9 x 16.2 x 9.81 mm

Ordering Information

Part Number	Package Type
PAT9102DM-T4QU	16-pin DIP Package
LM19-LSI	Lens

RoHS compliant

For any additional inquiries, please contact us at
http://www.pixart.com/contact.asp

1.0 Signal Description

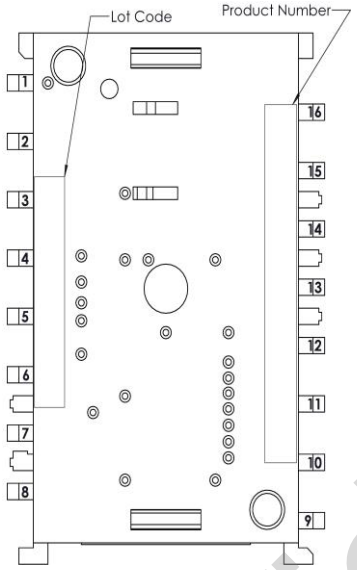


Figure 1. Pin Configuration

Table 1. PAT9102 Signal Pins Description

Pin No.	Signal Name	Type	Description
Functional Group:		Power Supplies	
4	VDDA28	Power	Internal voltage output @ 2.8V
5	VDDA25	Power	Internal voltage output @ 2.5V
6	VDDD18	Power	Internal voltage output @ 1.8V
7	VDDIO	Power	I/O reference voltage
15	VDD	Power	Input power supply
16	VLED	Power	Supply to LED anode
1	LED_GND	Ground	LED Ground
2	AGND	Ground	Analog ground
8	DGND	Ground	Digital ground
Functional Group:		Control Interface	
9	NCS	Input	Chip select
10	MOSI	Input	Serial data input
11	MISO	Output	Serial data output
12	SCLK	Input	Serial data clock
Functional Group:		Functional I/O	
13	NRST	Input	Hardware reset
14	MOTION	Output	Motion interrupt
Functional Group:		Data Interface	
3	NC	NC	No connection (float)

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Supply Voltage	V_{DD}	-0.5	3.7	V	
	V_{DDIO}	-0.5	3.7	V	
	V_{LED}	-0.5	3.7	V	
Input Voltage	V_{IN}	-0.5	V_{DDIO} + 0.5	V	All I/O pins
ESD	ESD_{HBM}		2	kV	All pins (Human Body Model)

Notes:

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
3. Functional operation should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	Including supply noise
	V_{DDIO}	3.0	3.3	3.6	V	Including supply noise
	V_{LED}	3.0	3.3	3.6	V	Including supply noise
Power Supply Noise				100	mV_{p-p}	At the supply point to the chip
Serial Port Clock Frequency	f_{SCLK}			2	MHz	50% duty cycle
Distance from Lens Reference Plane to Tracking Surface	Z	2.10	2.40	2.70	mm	
Repeated Error	R		0.15		%	On white paper & photo paper at nominal height of 2.4mm @ 10 ips velocity over 25 mm travel distance @ 20 ips velocity over 50 mm travel distance
Speed	V			20	ips	Max constant velocity
Acceleration	A			4	m/s^2	Acceleration from stationary position
Resolution of motion report				17904	cpi	

Note: PixArt does not guarantee the performance of the system beyond the recommended operating condition limits.

2.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Current	I_{DD_RUN}		22		mA	Average current consumption, including LED[2] current with 1ms polling.
Power Down Current	I_{PD}		30		uA	
Input Low Voltage	V_{IL}			0.3* V_{DDIO}	V	SCLK, MOSI, NCS
Input High Voltage	V_{IH}	0.7* V_{DDIO}			V	SCLK, MOSI, NCS
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS
Input Leakage Current	I_{LEAK}		± 1	± 10	uA	V_{in} = V_{DDIO} or 0V, SCLK, MOSI, NCS
Output Low Voltage	V_{OL}			0.45	V	I_{OUT} = 1mA, MISO, MOTION
Output High Voltage	V_{OH}	V_{DDIO} - 0.45			V	I_{OUT} = -1mA, MISO, MOTION

Notes:

1. All the parameters are tested under operating conditions: V_{DD} = 3.3V, V_{DDIO} = 3.3V, V_{LED} = 3.0V, Internal Clock = 80 MHz, Internal Slow Clock = 1 kHz, T_A = 25°C.
2. Typical pulse current drawn by V_{LED} is 55 mA.

2.4 AC Characteristics

Table 5. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Motion Delay After Navigation Start	$t_{MOT-NAV}$	35			ms	From navigation engine start to valid motion, assuming motion is present
Shutdown	t_{STDWN}			1.5	ms	From Shutdown mode active to low current
Wake from Shutdown	t_{WAKEUP}	5			ms	From Shutdown mode inactive to ready to accept IO command. Notes: A RESET must be asserted after a shutdown. Refer notes in section "**Error! Reference source not found.** Power-Down Sequence", also note $t_{MOT-NAV.}$
MISO Rise Time	t_{r-MISO}		50		ns	C_L = 100pF
MISO Fall Time	t_{f-MISO}		50		ns	C_L = 100pF
MISO Delay After SCLK	$t_{DLY-MISO}$			170	ns	From SCLK falling edge to MISO data valid, with 100pF load
MISO Hold Time	$t_{hold-MISO}$	200			ns	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	180			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time Between Write And Read Commands	t_{SWR}	180			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI Time Between Read And Subsequent Commands	t_{SRW} t_{SRR}	20			µs	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.

SPI Read Address-Data Delay	t_{SRAD}	160			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
SPI Read Address-Data Delay for Burst Mode Motion Read	t_{SRAD_MOTBR}	35			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read. Applicable for Burst Mode Motion Read only.
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS To SCLK Active	$t_{NCS-SCLK}$	120			ns	From last NCS falling edge to first SCLK rising edge
SCLK To NCS Inactive (For Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK To NCS Inactive (For Write Operation)	$t_{SCLK-NCS}$	35			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS To MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION Rise Time	$t_{r-MOTION}$		50		ns	C_L = 100pF
MOTION Fall Time	$t_{f-MOTION}$		50		ns	C_L = 100pF
Input Capacitance	C_{in}		50		pF	SCLK, MOSI, NCS
Load Capacitance	C_L			100	pF	MISO, MOTION
Transient Supply Current	I_{DDT}			33	mA	Max supply current during the supply ramp from 0V to VDD with min 150 us and max 20 ms rise time. (Does not include charging currents for bypass capacitors)
	I_{DDTIO}			50	mA	Max supply current during the supply ramp from 0V to VDDIO with min 150 us and max 20 ms rise time. (Does not include charging currents for bypass capacitors)

Note: All the parameters are tested under operating conditions: V_{DD} = 3.3V, V_{DDIO} = 3.3V, T_A = 25°C.

3.0 Mechanical Specifications

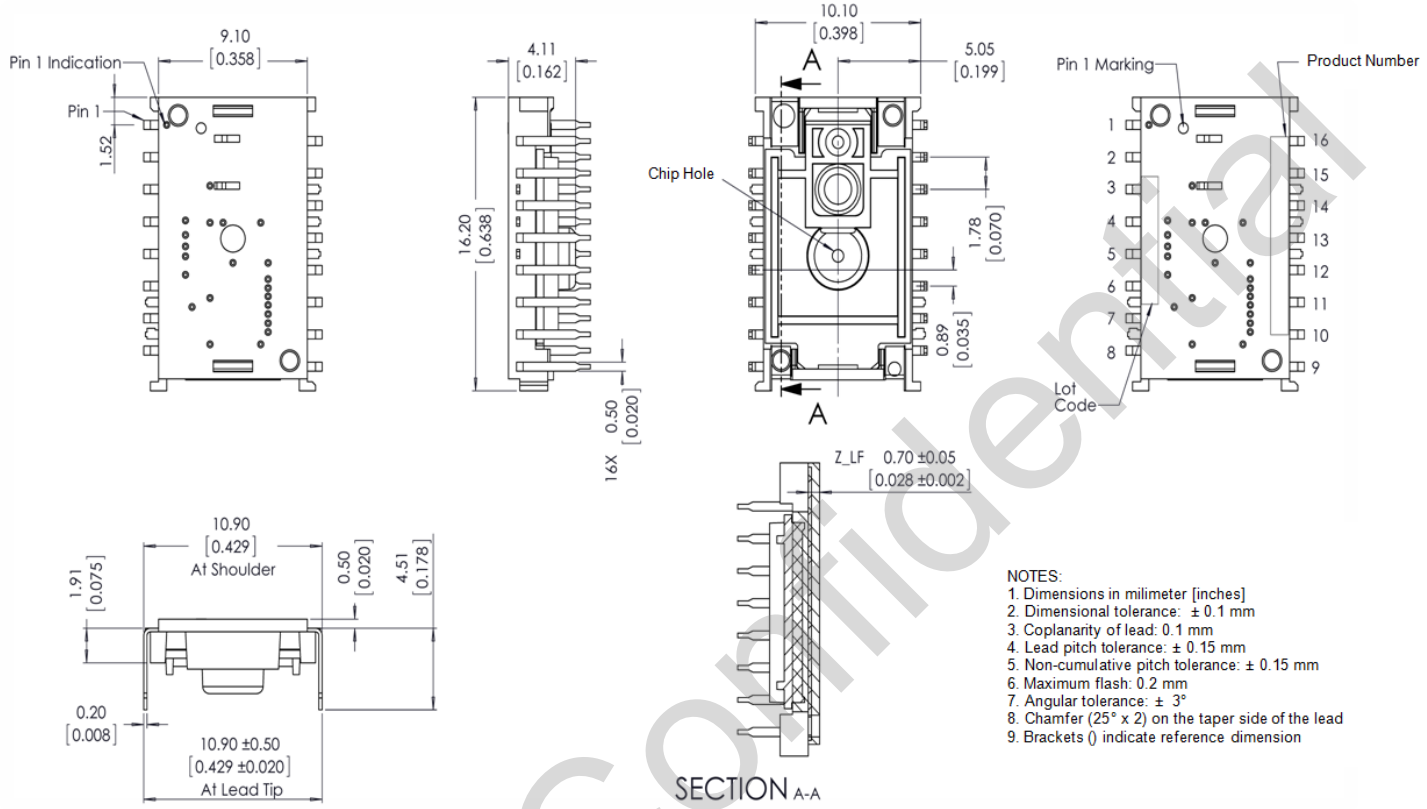
3.1 Package Marking

Refer to Figure 1. Pin Configuration for the code marking location on the device package.

Table 6. Code Identification

Code	Marking	Description
Product Number	PAT9102DM-T4QU	Chip part number label
Lot Code	AYWWXXXXXX	A: Assembly House Y: Year WW: Week XXXXXX: Reserved as PixArt reference

3.2 Package Outline Drawing



CAUTION: It is advised that normal static discharge precautions be taken in handling and assembling of this component to prevent damage and/or degradation which may be induced by ESD.

Figure 2. Package Outline Drawing

3.3 Assembly Drawings

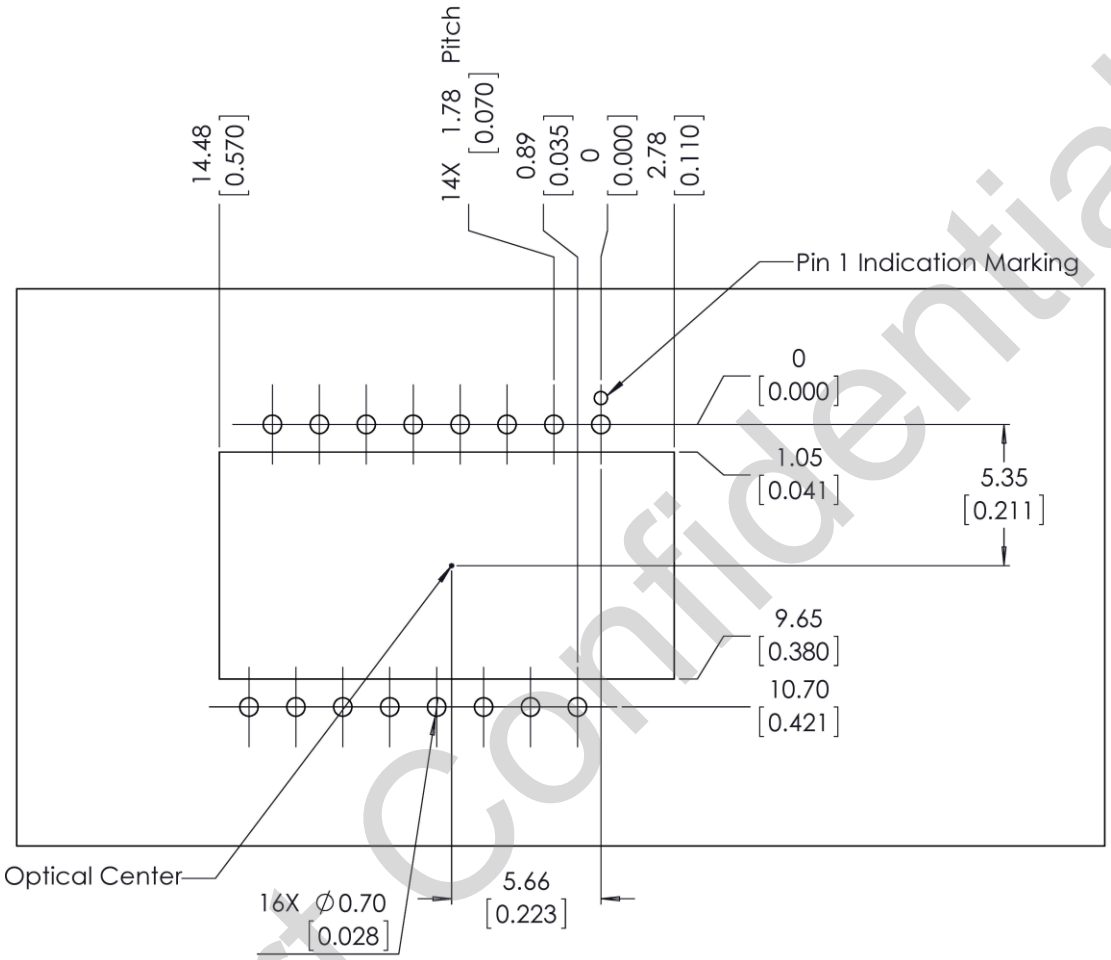


Figure 3. Recommended Chip Orientation, Mechanical Cutouts and Spacing (Top View)

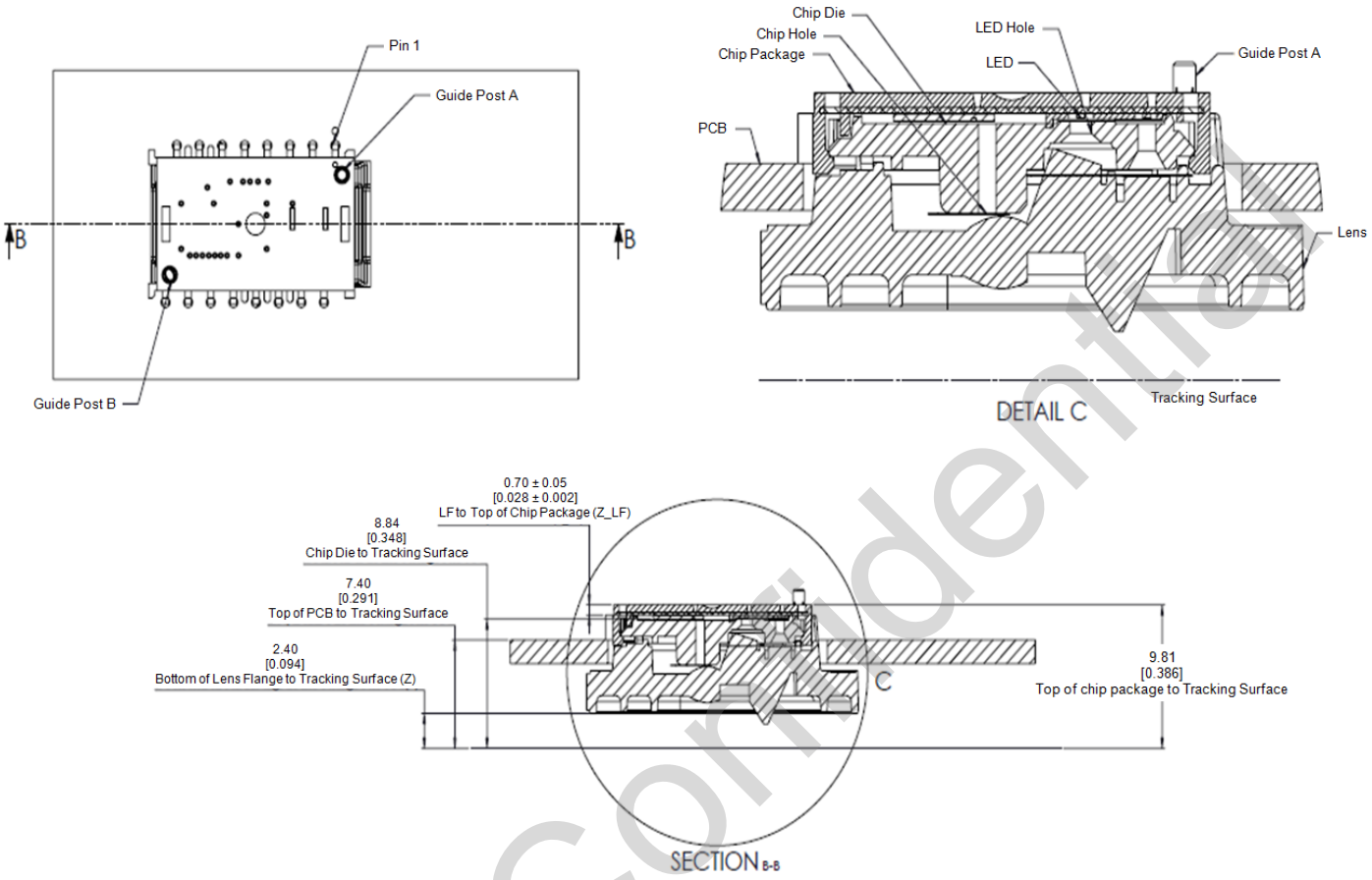


Figure 4. System Assembly View

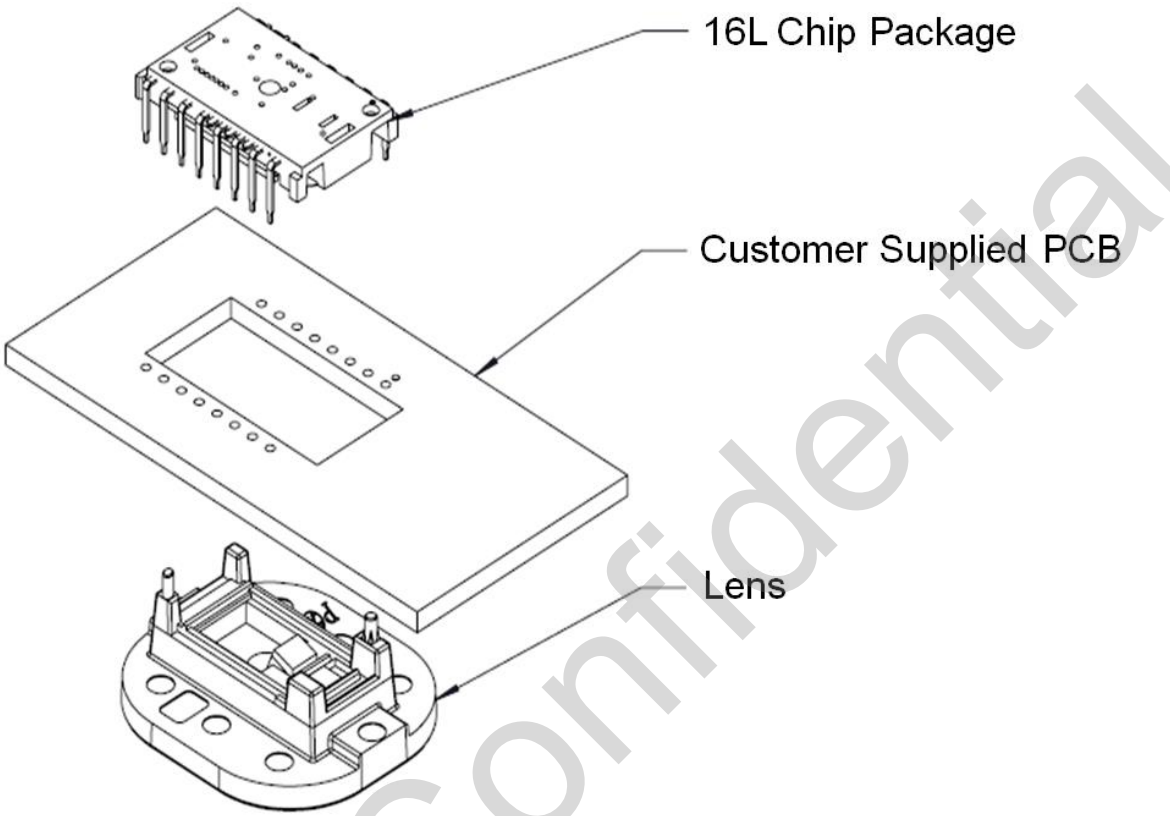


Figure 5. Exploded View of Assembly

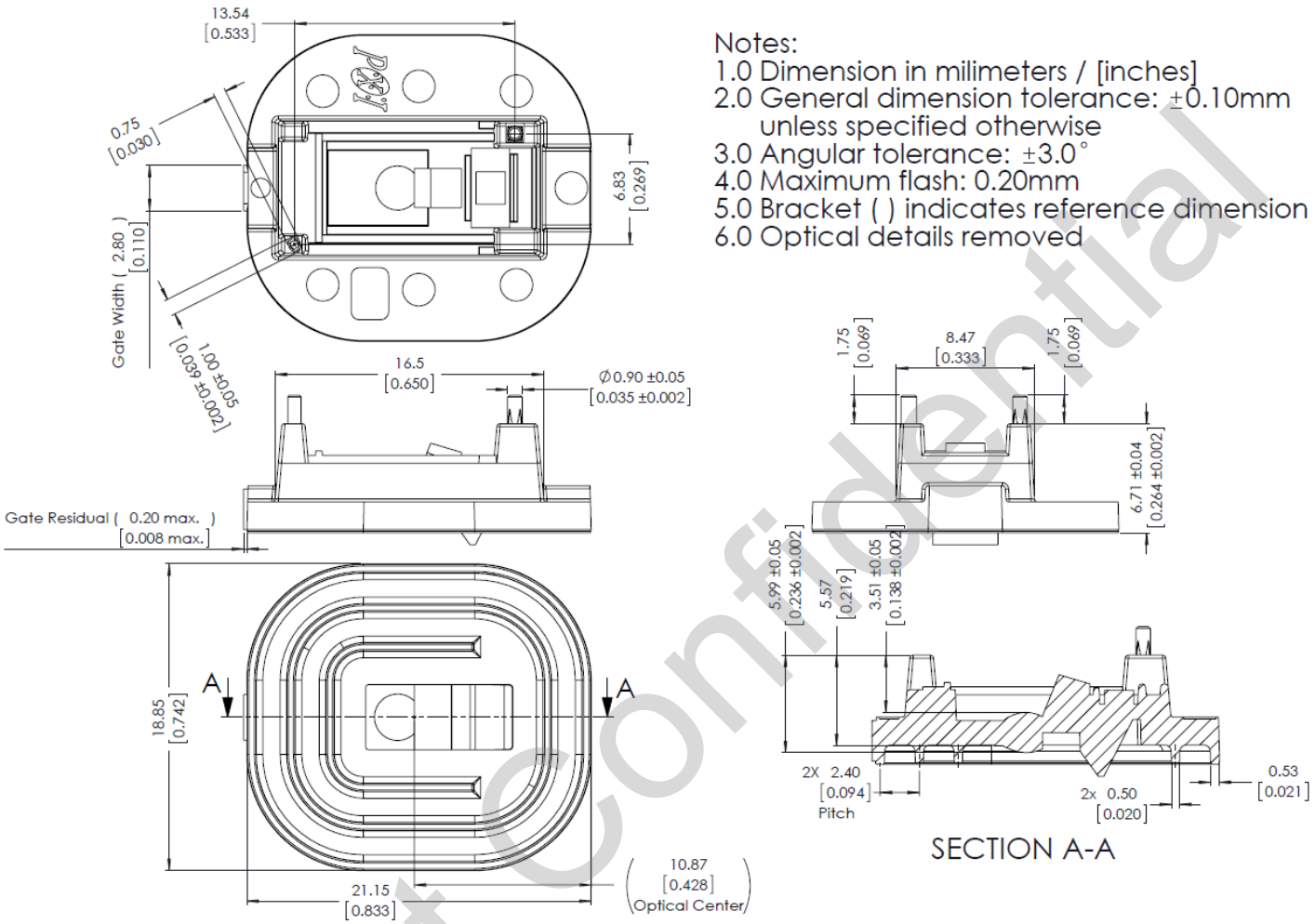


Figure 6. Lens Outline Drawing

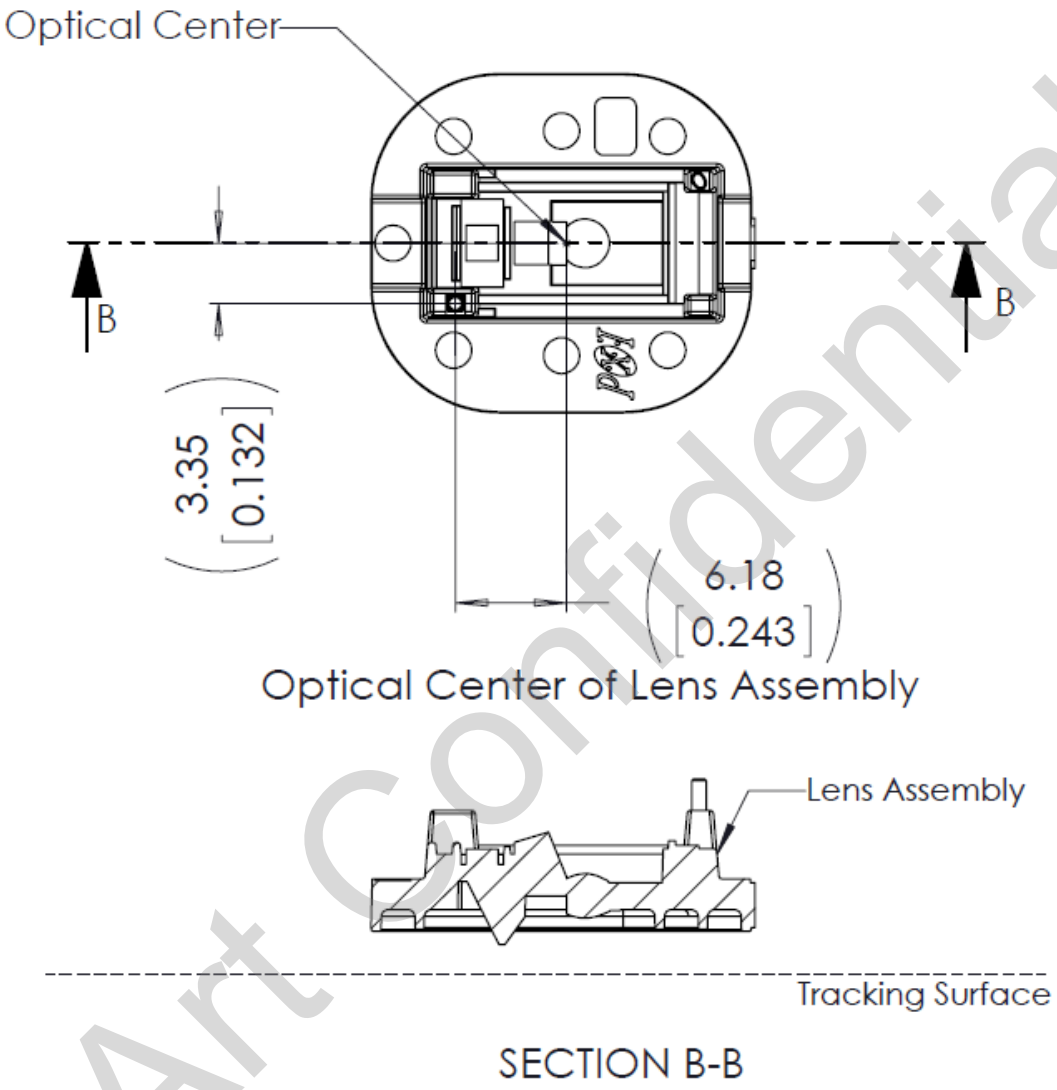


Figure 7. Cross Section View of Lens Assembly

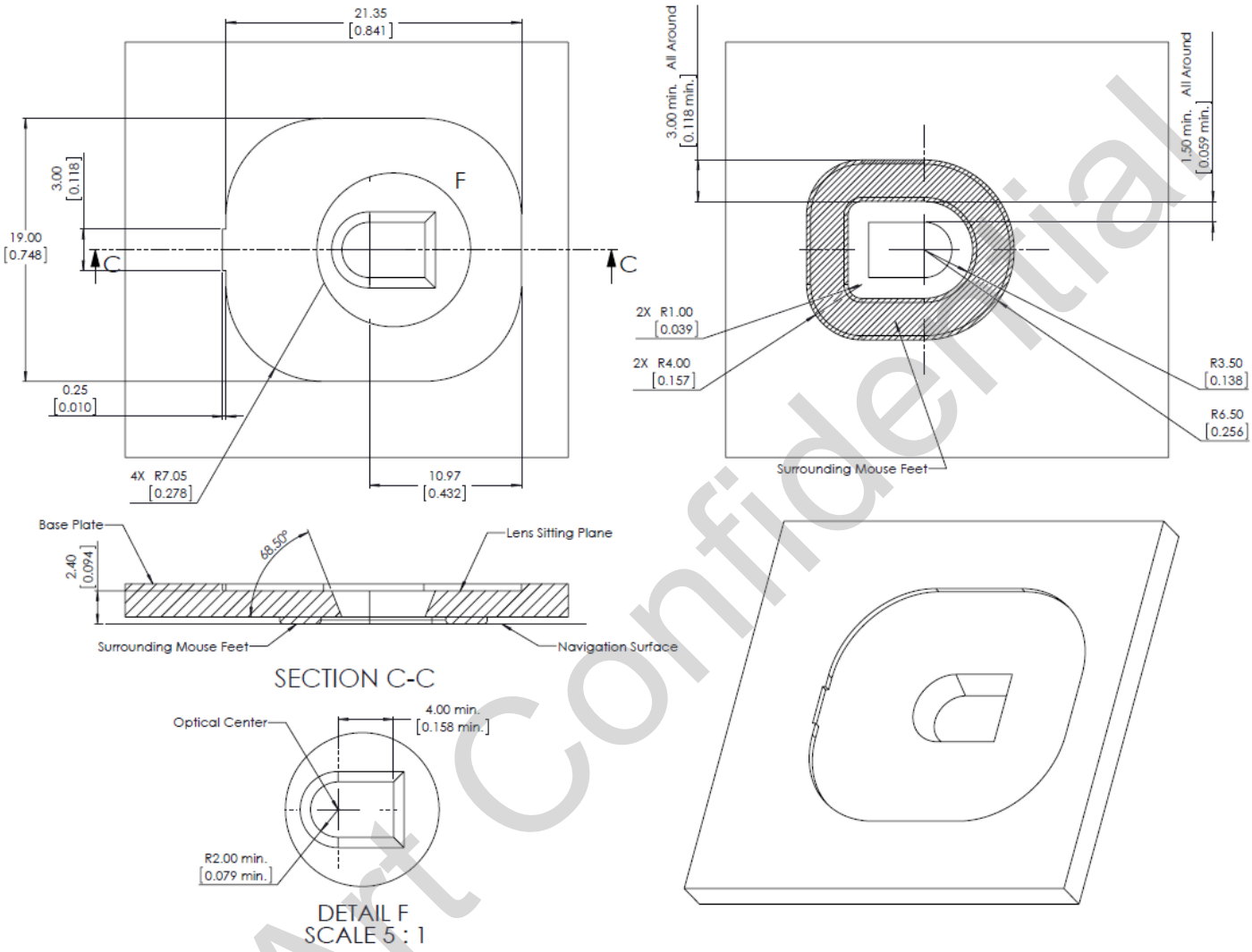
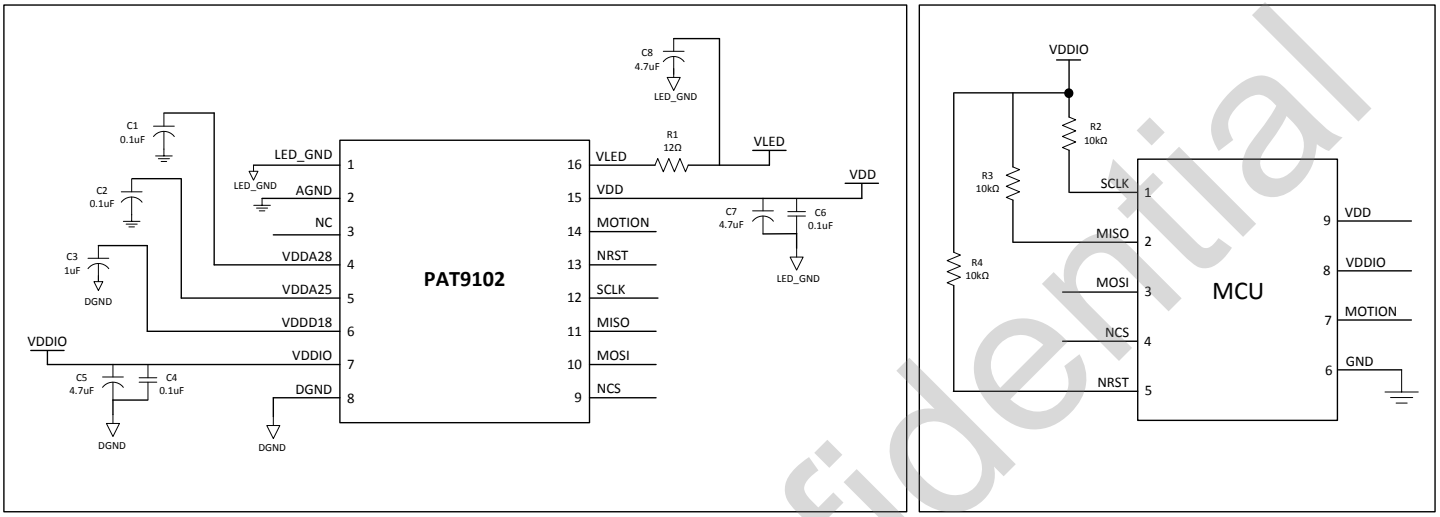


Figure 8. Recommended Base Plate Design

4.0 System Level Description

4.1 Reference Schematic



Note:
1. Capacitors must be placed near the chip.
2. LED's orientation is placed towards the palm of a hand.

External Component Type for PAT9102	Value	Quantity
Capacitor	0.1 uF	4
Capacitor	4.7 uF	3
Capacitor	1 uF	1
Resistor	12 Ω	1

Figure 9. PAT9102 Reference Schematics

4.2 Assembly Recommendation

- Insert the integrated chip and all other electrical components onto PCB.
- Wave-solder the entire assembly in a no-wash solder process utilizing solder-fixture. A solder-fixture is required to protect the chip from flux spray and wave solder.
- Avoid getting any solder flux onto the chip's body as there is potential for flux to seep into the chip package. The solder fixture should be designed to expose only the package leads to flux spray & molten solder while shielding the chip's body and optical apertures. The fixture should also set the chip at the correct position and height on the PCB.
- Place the lens onto the base plate. Care must be taken to avoid contamination on the optical surfaces.
- Remove the protective kapton tapes from optical apertures of the chip. Care must be taken to prevent contaminants from entering the apertures.
- Do not place the PCB with the chip facing up during the entire product assembly process.
  Note: Hold the PCB vertically when removing kapton tape.
- Insert PCB assembly over the lens onto the base plate's aligning post to secure PCB assembly in place. The chip package will self-align to the lens via the guide posts. The optical's reference position for the PCB is set by the base plate and lens.
- Recommendation: The lens can be permanently secured to the chip package by melting the lens' guide posts over the chip with heat staking process while maintaining pressing force of approximately 0.3kgf.

5.0 Registers

5.1 Registers List

PAT9102 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Table 7. Register List

Address	Register Name	Access	Reset	Address	Register Name	Access	Reset
0x00	Product_ID	RO	0xA0	0x13	SROM_Enable	R/W	0x00
0x01	Revision_ID	RO	0x02	0x14	Config2	R/W	0x08
0x02	Motion	RO	0x00	0x23	Config3	R/W	0x81
0x03	Delta_X_L	RO	0x00	0x25	Config5	R/W	0x04
0x04	Delta_X_H	RO	0x00	0x26	Observation	R/W	0x00
0x05	Delta_Y_L	RO	0x00	0x29	SROM_ID	RO	0x00
0x06	Delta_Y_H	RO	0x00	0x2E	Data_Out_Upper	RO	N/A
0x07	Squal_Upper	RO	0x00	0x2F	Data_Out_Lower	RO	N/A
0x08	Squal_Lower	RO	0x00	0x3A	Power_Up_Reset	WO	N/A
0x09	RawData_Sum_Upper	RO	0x00	0x3B	Shutdown	WO	N/A
0x0A	RawData_Sum_Lower	RO	0x00	0x3F	Inverse_Product_ID	RO	0x5F
0x0B	Maximum_RawData	RO	0x00	0x50	Motion_Burst	R/W	0x00
0x0C	Minimum_RawData	RO	0xFF	0x5E	Config6	R/W	0x12
0x0D	Shutter_Upper	RO	0x90	0x62	SROM_Load_Burst	WO	N/A
0x0E	Shutter_Lower	RO	0x01	0x64	RawData_Burst	R/W	0x00
0x12	Frame_Capture	R/W	0x00				